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PATENT NUMBER

U.S. UTILITY Patent Application

o.o. OTILITI I atom Applic	ation	
O.I.P.E.	PATENT DATE	
SCHNED NO 4 QA W		€ 6

APPLICATION NO. CONT/PRIOR CLASS SUBCLASS **ART UNIT EXAMINER** 09/940472 327 2816 Katsuji Kimura Linear voltage subtractor/adder circuit and MOS differential amplifier circuit therefor

ISSUING CLASSIFICATION								
ORIGINAL		CROSS REFERENCE(S)						
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TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED		
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.	
☐ The term of this patent				NOTICE OF ALL	OWĂNCE MAILED	
subsequent to (date) has been disclaimed.	(Assistant E	xaminer) ,	- (Date)			
The term of this patent shall	ę ·					
not extend beyond the expiration date of U.S Patent. No.				ISSUE FEE		
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this patent have been disclaimed.					•	
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WARNING:						
The information disclosed herein may be res Possession outside the U.S. Patent & Traden					5, Sections 122, 181 and 368.	

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